21. (Amended) The method of Claim 18 wherein the opening has an aspect ratio of at least 1.3.

23. (Amended) The method of Claim 8 wherein:

the body comprises an erasable programmable read-only memory region; and

the cobalt silicide layer is formed to contact a doped silicon section of the erasable programmable read-only memory region.--

Enclosed is Appendix B which shows how the above version of Claims 17, 20, 21, and 23 has been produced from the previous version of those claims. In Appendix B, added material is in bold, and deleted material is in brackets.

Add new Claims 26 - 35 as follows:

--26. The method of Claim 23 wherein the doped silicon section comprises doped monocrystalline silicon.

27. The method of Claim 8 wherein:

the body comprises (a) a doped monocrystalline silicon substrate, (b) a floating gate overlying the substrate, (c) a control gate overlying the floating gate, and (d) electrically insulating material which surrounds the floating gate and separates the gates from each other and from the substrate; and

the cobalt silicide layer is formed to contact the substrate.

28. The method of Claim 27 wherein:

the substrate comprises a pair of source/drain regions and a body region that (a) separates the source/drain regions from each other and (b) forms a pn junction with each source/drain region, the floating gate extending partially over at least one of the source/drain regions;

the cobalt silicide layer is formed to contact one of the source/drain regions.

29. The method of Claim 28 wherein a floating-gate transistor of a memory cell of an erasable programmable read-only memory is comprised by the regions and gates.

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30. The method of Claim 28 wherein the floating gate extends partially over only one of the source/drain regions.

31. The method of Claim 28 further including:

forming a further cobalt layer over the other of the source/drain regions;

forming a further titanium layer over the further cobalt layer by ionized physical vapor deposition;

reacting cobalt of the further cobalt layer with silicon of that other of the source/drain regions to form a further cobalt silicide layer; and

substantially removing the further titanium layer and any unreacted cobalt of the further cobalt layer.

32. The method of Claim 27 wherein the body includes (a) a select gate overlying the substrate generally lateral to the floating gate and (b) electrically insulating material which separates the select gate from the other gates and from the substrate.

33. The method of Claim 32 wherein:

the substrate comprises a pair of source/drain regions and a body region that (a) separates the source/drain regions from each other and (b) forms a pn junction with each source/drain region, the floating gate extending partially over one of the source/drain regions, the select gate extending partially over the other of the source/drain regions; and

the cobalt silicide layer is formed to contact one of the source/drain regions.

34. The method of Claim 33 wherein a floating-gate transistor of a memory cell of an erasable programmable read-only memory is comprised by the regions and gates.

35. The method of Claim 33 further including:

forming a further cobalt layer over the other of the source/drain regions;

forming a further titanium layer over the further cobalt layer by ionized physical vapor deposition;

reacting cobalt of the further cobalt layer with silicon of that other of the source/drain regions to form a further cobalt silicide layer; and

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substantially removing the further titanium layer and any unreacted cobalt of the further cobalt layer.--

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